SEMICONDUCTOR WAFER HAVING A BOTTOM SURFACE PROTECTIVE COATING

CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. patent application Ser. No. 08/517,603 filed Aug. 22, 1995 entitled, "Thermally Enhanced Micro-Ball Grid Array Package" by Rajeev Joshi having assignment rights in common with the present invention, which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates generally to integrated circuit (IC) devices and, more particularly, to a semiconductor wafer having a bottom surface that is coated with a protective coating prior to the performance of a wafer dicing, or die singulation, operation.

Currently, in order to remain competitive in the IC industry, IC process engineers must continuously increase device yield per wafer or lot. That is, process engineers seek to increase the number of usable semiconductor devices per wafer. Since any step in the fabrication process may detrimentally affect the IC device yield, process engineers seek to optimize each step and, as a result, reduce the number of lost IC devices for the optimized step.

For example, a conventional dicing, or sawing, process is one fabrication step that is likely to result in a substantial loss of devices. In general, when a wafer is diced, chipping may occur along the dicing edges of the individual IC devices. This chipping may then lead to the formation of cracks throughout the IC device, which cracking may damage the IC device and make the IC device unusable for its intended application. In other words, the chipping results in IC devices that are more vulnerable to stress and more susceptible to damage. As a result of an increase in unusable IC devices due to chipping, the IC device yield per wafer or lot is significantly reduced, and product reliability is compromised.

One type of IC device that may be chipped during the dicing operation is a flip chip device. During the dicing process, the flip chip device is cut away from the other flip chip devices of the wafer. The separated flip chip device may have, for example, rough edges as a result of the dicing process. After the flip chip device is separated from the other flip chip devices, the flip chip device is then packaged and/or mounted to a printed circuit board. As a result of chipping, the flip chip device may suffer various form of damage at any point subsequent to the dicing process. For example, the flip chip device may be damaged while it is being handled prior to mounting or packaging.

FIG. **1** is a side view of a conventional flip chip type device **100**. The flip chip **100** includes a die **102** that typically has a plurality of conventionally fabricated IC device structures. These IC device structures may include, for example, transistors and interconnect layers. The die **102** has a top surface **108** that includes bump pads (not shown). Bumps **106** are formed on the bump pads of the top most surface **108**. This top surface **108** is opposite a bottom surface **104** of the die **102**. The bottom surface **104** is conventionally left bare, or exposed. For example, the bottom surface **104** is bare silicon.

There are many problems associated with a conventional wafer that has conventional devices with exposed bottom surfaces. For example, one problem is the aforementioned

chipping during the dicing operation. That is, the exposed bottom surface fails to provide sufficient mechanical protection under certain stress inducing conditions. The exposed bottom surface also fails to provide protection from electrostatic shock or light induced bias for flip chip applications. That is, the devices may have functional problems due to photogenerated carriers when the bottom surface (e.g., **104**) of the die (e.g., **102**) is exposed to light, or the devices may be subject to an undesirable electrostatic shock during handling of the device subsequent to the dicing operation.

The aforementioned problems all contribute to a decrease in production yield. Consequently, there is a need for an improved wafer that provides a solution to the aforementioned problems. For example, there is a need for an improved wafer that is less susceptible to mechanical stress during and after a dicing operation. Additionally, there is a need for a method for making such an improved wafer.

SUMMARY OF THE INVENTION

To achieve the foregoing and other objects and according to the purpose of the present invention, a packaged integrated circuit device is disclosed. The device includes a die having a plurality of electrical contacts on a first surface of the die and a protective film adhered directly to a back surface of the die, the protective film being thick enough to allow laser marking of the protective film without the laser penetrating to the die. In one preferred embodiment, the protective film of the device is a thick film formed by screen printing. In a preferred embodiment, the protective film has a thickness of between about 1.5 and 5 mils.

In another embodiment, a semiconductor wafer is disclosed. The wafer includes a multiplicity of semiconductor dies, and each die has a plurality of electrical contacts that are exposed on a first surface of the wafer. The wafer further includes a protective thick film adhered directly to a second surface of the wafer. The protective film is thick enough to allow laser marking of the protective film without the laser penetrating to the die.

In another aspect of the invention, a method of fabricating a semiconductor wafer having a wafer substrate with a top surface and a bottom surface and a plurality of dies is disclosed. The method includes providing a plurality of dies on the top surface of the wafer substrate. A plurality of electrical contacts are disposed on each die. The method further includes printing a thick film upon the bottom surface of the wafer substrate such that the thick film is thick enough to allow laser marking of the thick film without the laser penetrating to one of the plurality of dies. In a preferred embodiment, the printing act includes placing a screen across the bottom surface of the wafer substrate, where the screen has a first end and a second end that is opposite the first end, depositing a predefined amount of material at the first end of the screen, and dragging a squeegee from the first end to the second end of the screen such that the material is thinly deposited through the screen and across the bottom surface of the wafer substrate to form the thick film. In another preferred embodiment, the method further includes adhering a mounting tape to the thick film, and dicing the wafer such that the dies are separated from each other. The mounting tape is not an especially adhesive type tape.

In another embodiment, a method of fabricating a semiconductor wafer having a wafer substrate with a top surface and a bottom surface and a plurality of dies is disclosed. In this embodiment, the method includes providing a plurality of dies on the top surface of the wafer substrate, applying a

thick film over the bottom surface of the wafer substrate, adhering the thick film to a mounting tape that is a UV type tape, and dicing the wafer to separate the dies. In this embodiment, the thick film reduces chipping along edges of the separated dies.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. **1** is a diagrammatic side view of a conventional flip chip type device.

FIG. **2** is a diagrammatic side view of a flip chip device in accordance with one embodiment of the present invention.

FIG. **3** is a diagrammatic representation of a bottom surface of a flip chip device that illustrates a substantial reduction in chipping as a result of the application of a thick film to a portion of the bottom surface in accordance with one embodiment of the present invention.

FIG. **4** is a diagrammatic top view of a wafer that includes a plurality of flip chip devices of FIG. **2** in accordance with one embodiment of the current invention.

FIG. **5** is a flowchart illustrating the process of fabricating a flip chip bumped wafer that includes screen printing a thick film in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Methods and apparatus for protecting IC devices of a wafer during and after a dicing operation are described below. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order not to unnecessarily obscure the present invention.

In general, the present invention includes a wafer having a protective film for substantially preventing damage to the dies of the wafer during and after the dicing process. For example, the protective film substantially prevents chipping along the dicing edges of the dies. Although the following description is in reference to flip chip devices, of course, it should be well understood to those skilled in the art that the present invention is not limited to flip chip devices, but may be implemented on any device that has an exposed bottom surface during the dicing process, such as a flash memory device or a chip size package (CSP). One example of a CSP is a ball grid array package type, which package type is described in U.S. patent application Ser. No. 08/517,603 (Attorney Docket No. NSC1P073) filed Aug. 22, 1995 entitled, "Thermally Enhanced Micro-Ball Grid Array Package" by Rajeev Joshi having assignment rights in common with the present invention, and which is herein incorporated by reference.

FIG. **2** is a side view of a flip chip device **200** in accordance with one embodiment of the present invention. The flip chip **200** includes a die **102** that typically has a plurality of conventionally fabricated IC device structures. These IC device structures may include, for example, transistors and interconnect layers. The die **102** has a top surface **108** that includes a plurality of electrical contacts (not shown). Bumps **106** are formed on the electrical contacts of the top most surface **108**. This top surface **108** is opposite a bottom surface **104** of the die **102**. In this embodiment, a protective film **210** is applied to the bottom surface **104** of the die.

The protective film **210** may be formed from any suitable material. For example, the protective film may be formed from a plastic material or epoxy. By way of example, Encapsulant EO 1016 from Dexter Hysol works well. This epoxy is commonly also used as a glob top material for chip-on-board applications that protects the die and wire bonds. The protective film may have any thickness that substantially prevents chipping during the dicing operation and is suitable for the particular application. For example, the protective film may have a thickness that allows laser marking of the thick film without the laser penetrating the thick film. Preferably, the protective film is between about 1.5 and 5 mils. Most preferably, the protective film is between about 2 and 3 mils.

FIG. **4** is a top view of a wafer **400** that includes a plurality of flip chip devices **200** of FIG. **2** in accordance with one embodiment of the current invention. As shown, the flip chip devices **200** are formed on the wafer **400** in an array pattern. Scribe lines **402** are positioned between each flip chip device **200**. When the wafer is diced, the dicing tool cuts along the scribe lines **402**, which dicing process is described in detail below in reference to FIG. **5**.

A protective film (shown in FIG. **2** as **210**) is deposited over the bottom surface of the wafer **400**. The top surface of the wafer is opposite the bottom surface. A plurality of electrical contacts may be disposed on the top surface. Additionally, bumps (not shown) may be deposited on the electrical contacts. The protective film **210** of the bottom surface aids in preventing chipping during the wafer dicing process. Preferably, the protective film **210** is in the form of a thick film, and is formed by any suitable process for applying a thick film. In one embodiment, a screen printing process is utilized. By way of another example, a spinning type process may be used, wherein a thick film is spread across the bottom surface of the wafer.

FIG. **5** is a flowchart illustrating the process **500** of fabricating a flip chip bumped wafer that includes screen printing a thick film in accordance with one embodiment of the present invention. Initially, a plurality of dies are provided on a top surface of a wafer substrate in operation **501**. As mentioned above, each die includes a plurality of electrical contacts. Next, in operation **502**, a plurality of bumps may be deposited on the electrical contacts of each die. The top surface is opposite a bottom surface of the wafer substrate. The dies are formed by depositing a plurality of layers on the top surface of the wafer substrate. The dies may include IC devices such as transistors. The plurality of layers are deposited by conventional fabrication techniques.

After a plurality of dies are provided, in operations **503** through **505** a thick film is printed onto the bottom surface of the wafer substrate. The thick film is applied by any application technique that is suitable for applying a thick film. For example, operations **503** through **505** describe a screen printing process. The screen printing process includes operation **503**, in which a screen is placed over the bottom surface of the wafer substrate. Next, in operation **504** a predefined amount of material is deposited at a first end of the screen. In operation **505**, a squeegee is dragged from the first end to the opposite end of the screen. As the squeegee is dragged across the screen, the material is deposited